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(54) Name of Invention Semiconductor device
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Detailed Description

1. Name of invention
Semiconductor device

2. Scope of Claim for Patent
(1) A semiconductor device comprising a second semiconductor substrate laminated through an insulating film onto a first semiconductor substrate, and elements and portions of elements formed on the upper surfaces of said first and second semiconductor substrate, and having at least the element separation area of said first semiconductor substrate assured by means of a portion of the element separation area formed on said second semiconductor substrate.

(2) The semiconductor device according to claim 1, wherein said element separation area is formed by a trench opened in a semiconductor substrate and an insulative film filling said trench.

3. Detailed Description of Patent

[Overview]
A semiconductor device wherein transistors, resistors etc. forming digital and analog circuits are formed on the upper surface of a second semiconductor substrate, whereas the areas of impurities forming the necessary capacitance for analog circuits are formed on the upper surface of a first semiconductor substrate, and the said second semiconductor substrate is laminated onto the top of the first semiconductor substrate through an insulating film, and thereby forming analog circuits that are not easily affected by noise

generated by the digital circuits because the digital circuits and analog circuits can be easily separated, and that is also capable of high integration resulting from the ability to form the necessary capacitors for analog circuits on another substrate but formed below the element area, and further capable of high speed and high reliability resulting from the ability to be formed on low-density silicon substrates and by SOI.

[Field of use in industry]

The present invention pertains to a semiconductor device related to MIS type semiconductor devices, particularly semiconductor devices capable of forming semiconductor integrated circuits requiring high integration capacity.

Previously, in semiconductor integrated circuits requiring highly integrated capacitance, insulative films for capacitance were normally formed as thin films, but in the present day of extremely thin films the limits of voltage resistance and leak characteristics etc. of insulative films are being approached and further reduction in film thickness is difficult. Also, methods using trench capacitors or stack type capacitors above the element area are capable of forming capacitors in a comparatively small area, but present problems in terms of precision and noise characteristics, and are therefore difficult to use in analog circuits. Forming capacitors with good precision that is not subject to the effects of noise means forming [capacitors] in an inactive field area away from the area where elements are formed, and therefore requires an extremely large area, a capacitor area that is far larger than the other elements (transistors, resistors, etc.) and [therefore] poses the significant problem of being an obstacle to integration. For this reason, there is demand for a means of forming highly integrated capacitors with excellent precision and strong resistance to noise.

[Prior art]

Figure 4 shows a cross sectional view of a semiconductor device according to prior art, being a digital-analog hybrid C-MOS type semiconductor device. 51 is an n-type silicon (Si) substrate, 52a is a p- type well area in the digital block, 52b is a p- type well area in the analog block, 53 is a p- type channel stopper area, 54 is an n- type channel stopper area, 55 is a field oxide layer, 56a and 56b are n+ type source/drain areas, 56c is an n+ type substrate contact area (not shown in the drawing), 57a and 57b are p+ type source-drain areas, 57c is a p+ type well connector area in the digital block, 57d is a p+ type well connector area in the analog block, 58 is a gate oxide layer, 59 is a gate electrode, 60 is a lower-layer electrode in the capacitor block, 63 is a block oxide film, 64 is a phosphosilicate glass (PSG) film, and 65 is Al wiring.

In the same drawing, p- type well area 52a for the digital block and p- type well area 52b for the analog block are selectively divided using n- type silicon (Si) substrate 51, each respectively forming N-channel transistors, forming digital and analog P-channel transistors on n- type silicon (Si) substrate 51, and forming capacitors in insulative film 61 sandwiched between two semiconductors (60, 62) on a field oxide film where no elements are formed. Because the digital ground and analog ground are divided into different p- type well areas (52a, 52b), the circuits configured in the analog block are generally not susceptible to the effects of noise created in the digital circuit block, but because both p- type well areas (52a, 52b) are formed in common on n- type silicon (Si) substrate 51, the noise improvement is not perfect. Also, the fact that the grounds are formed using p- type

well areas makes it necessary to use an n- type silicon (Si) substrate, and this makes faster speeds difficult because it is not possible to use a low-density p- type silicon (Si) substrate. Further, because the capacitor block is formed on a field oxide film where no elements are formed, the degree of integration is not improved.

[Problems resolved by the invention]

The problems resolved by the present invention are the inability to form analog circuits that are not affected by noise generated in the digital circuit block, the inability to form high-speed digital-analog hybrid integrated circuits using low-density p- type silicon (Si) substrates, and the inability to form integrated circuits having highly integrated capacitors as described in the example of prior art.

[Means by which the invention resolves the problems]

The above problems are resolved by means of a semiconductor device according to the present invention, comprising a second semiconductor substrate laminated through an insulating film onto a first semiconductor substrate, and elements and portions of elements formed on the upper surfaces of said first and second semiconductor substrate, and having at least the element separation area of said first semiconductor substrate assured by means of a portion of the element separation area formed on said second semiconductor substrate.

[Operation]

Thus in a semiconductor device according to the present invention, transistors, resistors, etc. configuring digital and analog circuits are formed on the upper surface of the second semiconductor substrate, while the area of impurities for configuring the capacitor necessary for analog surfaces is formed on the upper surface of the first semiconductor substrate, and also the first semiconductor substrate is laminated through an insulating film onto said second semiconductor substrate, and is further formed in a structure in which the element separation area on the first semiconductor substrate is self-aligned with respect to a portion of the element separation area on the second semiconductor substrate. Accordingly, because the digital circuits and analog circuits can easily be separated, it is possible to configure analog circuits that are not affected by noise generated in the digital circuits. In addition, because the capacitors required by the analog circuit configuration are formed on a separate substrate, and also are formed below the transistors, resistors etc., it is possible to achieve high integration. And further, because it is possible to form transistors and resistors etc. of SOI, and on a low-density silicon substrate, it is possible to achieve high speed and high reliability. Thus it is possible to obtain a semiconductor device enabling the formation of semiconductor integrated circuits having extremely high performance, high speed and high reliability.

[Preferred embodiment]

Next we specifically describe the present invention in terms of the illustrated preferred embodiments. Figure 1 shows a schematic cross sectional view of a first preferred embodiment of a semiconductor device according to the present invention, Figure 2 shows a schematic cross sectional view of a second preferred embodiment of a semiconductor device according to the present invention, and Figure 3 (a) through (e) show a process cross sectional view of a preferred embodiment of a method of manufacturing a semiconductor device according to the present invention.

In all drawings, the same entities correspond to the same numbers.

Figure 1 shows a schematic cross sectional view of the first preferred example of a semiconductor device according to the present invention using a p- type silicon substrate in which 1 is a p- type first silicon (Si) substrate of approximately 10^{15} cm^{-3}, 2 is an n+ type impurity area of approximately 10^{20} cm^{-3}, 3 is an oxide film of approximately 1μm, 4 is a p- type second silicon (Si) substrate of approximately 10^{15} cm^{-3}, 5 is an n- type well area of approximately 10^{16} cm^{-3}, 6a and 6b are trench filling oxide layers, 7 is an n+ type source/drain area of approximately 10^{20} cm^{-3}, 8 is a p+ type source/drain area of approximately 10^{20} cm^{-3}, 9 is a gate oxide layer of approximately 20 nm, 10 is a gate electrode of approximately 300 nm, 11 is a side wall insulating film (chemical vapor growth oxide film), 12 is an embedded electrode (selective chemical vapor growth tungsten film), 13 is a block oxide layer of approximately 50 nm, 14 is a phosphosilicate glass (PSG) film or approximately 0.8 μm, and 15 is AI wiring of approximately 1 μm.

In the same drawing, p- type second silicon (Si) substrate 4 is laminated through oxide layer 3 onto p- type first silicon (Si) substrate 1 having n+ type impurity area 2 created on its upper surface. Trenches separating element areas are selectively created on p- type second silicon (Si) substrate 4, and some trenches have n+ type impurity areas 2 are created on silicon (Si) substrate 1 separated and self-aligned. All trenches are filled in with trench filling oxide layers (6a, 6b) forming a flat [surface]. The N-channel transistors of the digital and analog blocks respectively are formed on element areas separately defined on p- type second silicon (Si) substrate 4, and the P-channel transistors of the digital and analog blocks respectively are formed on n- type well areas 5 separately defined on formed on second silicon (Si) substrate 4. Below the N and P channel transistors, capacitors are formed comprising a PN junction between n+ type impurity area 2 insulated by oxide film 3, and p- type first silicon (Si) substrate 1. (Here the connection to n+ type impurity areas 2 formed in the upper surface of p- type first silicon (Si) substrate 1 uses the connection technology applied for in submission number 1-31902 as a result of the present invention.) Accordingly because the digital circuits and analog circuits can be separated as islands by an insulating film, it is possible to configure analog circuits that are not affected by noise generated in the digital circuits. Also, because the capacitors required by the analog circuit configuration can be formed on a separate substrate but below the element areas, it is possible to enable high levels of integration. Further, because all elements can be formed of SOI, and also on a low-density silicon substrate, it is possible to enable high speed and high reliability as well.

Figure 2 shows a schematic cross sectional view of a second preferred embodiment of a semiconductor device according to the present invention.

The configuration of the second preferred embodiment is essentially the same as the first preferred embodiment, but differs in that a larger capacitor is formed. [Numbers] 1 through 15 indicate the same items as in Figure 1, 16 is a thin-film insulating film for capacitor formation, 17 is a conductive film (tungsten silicide film), and 18 is a polycrystalline silicon film.

In the same drawing, in addition to the PN junction capacitor formed between n+ type impurity area 2 formed on p- type first silicon (Si) substrate 1 and p- type first silicon (Si) substrate 1, insulating film capacitors are formed in parallel rows directly above said n+ type impurity area 2, formed by sandwiching insulating film for capacitor formation 16 between said n+ impurity area 2 and an upper layer capacitor electrode formed by the two layers, tunsten silicide film 17 and polycrystalline silicon film 18, enabling the formation of extremely large capacitors.

Next, we describe one preferred embodiment of a means of manufacturing a semiconductor element according to the present invention, with reference to Figures 3(a) through (e) and Figure 1.

Figure 3(a)

Here n+ type impurity area 2 is formed by ion implantation onto p- type second silicon (Si) substrate 4, using normal photolithography technology, and nitride films and oxide films are formed on n+ type impurity area 2 to which connections are desired.

Figure 3(b)

Next, oxide film 3 is grown on the lower surface of p- type second silicon (Si) substrate 4 and laminated onto the top of the p- type first silicon (Si) substrate by annealing for approximately two hours at approximately 1100°C in a N2/O2 atmosphere. Then, second silicon (Si) substrate 4 is abraded to [thickness of] approximately 5μm.

Figure 3(c)
Next, oxide films and nitride films are grown in that order. (Not shown in the drawing, these two films are both stopper films filling in trench with oxide layers.) Then first, using normal photolithography technology, in order to form a first element separation area on a part of p- type second silicon (Si) substrate 4, a first trench is formed by opening a hole in the nitride film, oxide film, and p- type second silicon (Si substrate 4). Then, in order to form a second element separation area in a portion of p- type second silicon (Si) substrate 4 and an element separation area in p- type first silicon (Si) substrate 1, a second trench is formed by opening a hole in the nitride film, oxide film, p- type second silicon (Si) substrate 4, oxide film 3, and p- type first silicon (Si) substrate 1. Then, said second trench 2 is filled in with oxide film 6b. Here, the element separation area formed on the p- type second silicon (Si) substrate is formed by both the first trench and the second trench. (Note however that in the case that the element separation area formed on p- type second silicon

(Si) substrate 4 and the element area formed on p- type first silicon (Si) substrate 1) are identical, there is no need to divide the trench formation [process] into two cycles.) Then, using normal photolithography technology, n- type well area 5 is formed by phosphorus ion implantation using resist and trench filling oxide films (6a, 6b) as a mask layer.

Figure 3(d)
Next, using normal photolithography technology, holes are opened through the nitride film, oxide film, p- type second silicon (Si) substrate 4, and oxide film 3 on top of n+ impurity area 2 to which the connection is desired, exposing n+ type impurity layer 2. Then, a chemical vapor growth oxide film is grown, and anisotropic dry etching is performed leaving chemical vapor growth oxide film 11 on only the side walls of said holes. Then, selective chemical vapor growth tungsten film 12 is grown, filling in said holes and forming connections to n+ type impurity area 2. Then the nitride film and oxide film are removed by etching.

Figure 3(e)
Next, gate oxide film 9 and a polycrystalline silicon film are formed in that order. Then, using normal photolithography technology, the polycrystalline silicon film is formed by patterning into gate electrode 10. Then, using normal photolithography technology, n+ type source-drain areas 7 are formed by arsenic ion implantation and p+ type source-drain areas 8 are formed by boron ion implantation using resist, gate electrode 10 and trench filling oxide films (6a, 6b) as a mask layer.

Figure 1

Next, block oxide film 13, and phosphosilicate class (PSG) film 14 are formed in [that] order. Then, electrode contact windows and AI wiring 15 etc. are formed by applying normal technology, and the semiconductor device is completed.

In the first preferred embodiment, a capacitor is formed consisting of an area of impurities on the upper surface of p- type first silicon (Si) substrate 1, however it is also possible to form resistors consisting of an area of impurities. In that case, it is possible to form highly integrated digital-analog converters etc. using these resistors.

As shown in the above preferred embodiments, in a semiconductor device according to the present invention, because the digital circuits and analog circuits can easily be separated, it is possible to configure analog circuits that are not affected by noise generated in digital circuits. Also, because the capacitor necessary for configuring analog circuits are formed on a separate substrate but below the transistors and resistors, etc., it is possible to achieve high speed and high reliability.

[Effect of the invention]
As explained above, by means of the present invention, it is possible to achieve high speed and high reliability in an MIS type semiconductor device, because it is possible to configure elements on the upper surface of a first semiconductor substrate and the upper surface of a second semiconductor substrate through an insulating film, with high reliability resulting from the ability to form analog circuits that do not receive the effects of noise generated in digital circuits, and also high integration resulting from the ability to configure the capacitors necessary to configure analog circuits underneath the elements, and further the ability to form all elements of SOI on low-density polysilicon substrates. In other words it is possible to realize a semiconductor integrated circuit having high capacity, high reliability, and high integration at the same time.

4. Simplified explanation of drawings

Figure 1 is a schematic cross sectional drawing of the first preferred embodiment of a semiconductor device according to the present invention.

Figure 2 is a schematic cross sectional drawing of the second preferred embodiment of a semiconductor device according to the present invention.

Figure 3(a) through (e) are process cross sectional drawings of a preferred embodiment of the a manufacturing method for a semiconductor device according to the present invention.

Figure 4 is a schematic cross sectional drawing of a semiconductor device according to prior art.

In the drawings,

1 p- type first silicon (Si) substrate,
2 n+ type impurity area
3 oxide film
4 p- type second silicon (Si) substrate
5 n- type well area
6a, 6b trench filling oxide layers
7 n+ type source/drain area
8 p+ type source/drain area
9 gate oxide layer
10 gate electrode
11 side wall insulating layer (chemical vapor growth oxide film)
12 filling conductive film (selective chemical vapor growth tungsten film)
13 block oxide layer
14 phosphosilicate glass (PSG) layer
15 Al wiring
16 thin film insulative layer for capacitor formation
17 conductive film (tungsten silicide film)
18 polycrystalline silicon film

Takehide Shirado, Patent Applicant

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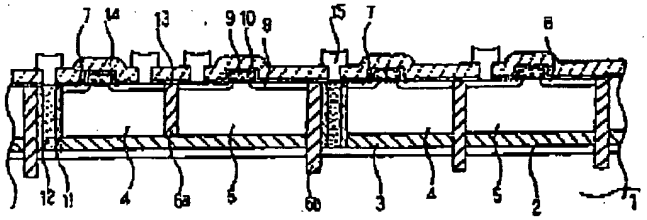
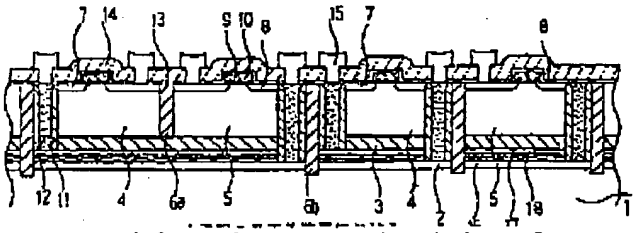


Schematic cross sectional view of a first preferred embodiment of a semiconductor device according to the present invention

Figure 1

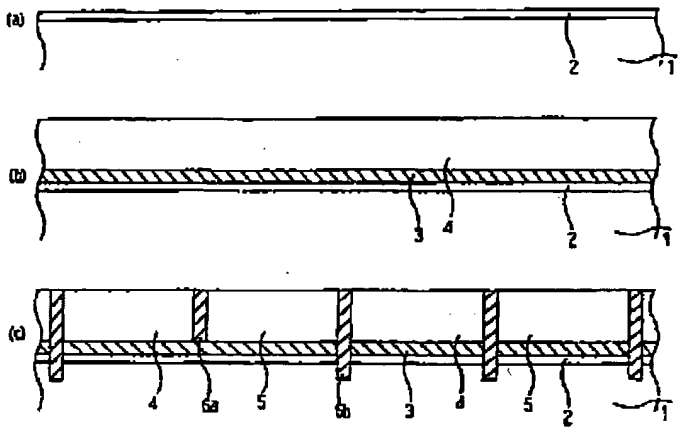
1	p- type first silicon (Si) substrate,	9	gate oxide layer
2	n+ type impurity area	10	gate electrode
3	oxide film	11	side wall insulating layer (chemical vapor growth oxide film)
4	p- type second silicon (Si) substrate	12	filling conductive film (selective chemical vapor growth tungsten film)
5	n- type well area	13	block oxide layer
6a, 6b	trench filling oxide layers	14	phosphosilicate glass (PSG) layer
7	n+ type source/drain area	15	AI wiring
8	p+ type source/drain area		



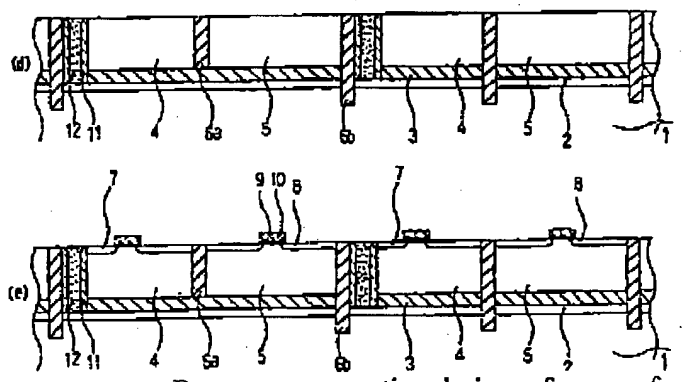
Schematic cross sectional view of a second preferred embodiment of a semiconductor device according to the present invention

Figure 2

1	p- type first silicon (Si) substrate,	11	side wall insulating layer (chemical vapor growth oxide film)
2	n+ type impurity area	12	filling conductive film (selective chemical vapor growth tungsten film)
3	oxide film	13	block oxide layer
4	p- type second silicon (Si) substrate	14	phosphosilicate glass (PSG) layer
5	n- type well area	15	AI wiring
6a, 6b	trench filling oxide layers	16	thin film insulative layer for capacitor formation
7	n+ type source/drain area	17	conductive film (tungsten silicide film)
8	p+ type source/drain area	18	polycrystalline silicon film
9	gate oxide layer		
10	gate electrode		



Process cross sectional view of one preferred embodiment
of a manufacturing method for a semiconductor device according to the present invention
Figure 3



Process cross sectional view of one preferred embodiment
of a manufacturing method for a semiconductor device according to the present invention
Figure 3

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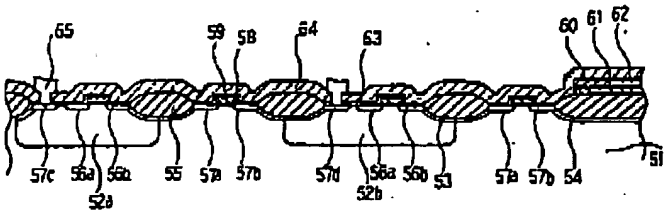

Schematic cross-sectional view
of a semiconductor device according to prior art
Figure 4